

# Radiation Effects of Commercial Resistive Random Access Memories

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# Acknowledgement

- **Sponsors:**
  - **NASA Electronics Parts and Packaging (NEPP) Program**
  - **Defense Threat Reduction Agency (DTRA)**
  - **National Reconnaissance Office (NRO)**
- **Adesto and Panasonic for providing technical support**



# Acronyms

- **1T1R** – 1 transistor 1 resistor
- **BEOL** – Back-end-of-line
- **CBRAM** – Conductive-bridge random access memory
- **CMOS** – Complimentary metal-oxide-semiconductor
- **EEPROM** – Electrically erasable programmable read only memory
- **LCDT** – Low cost digital tester
- **LBNL** – Lawrence Berkeley National Laboratory
- **LET** – Linear energy transfer
- **RAM** – Random access memory
- **ROM** – Read-only memory
- **ReRAM** – Reduction-oxidation random access memory
- **RRAM** – Resistive Random Access Memory
- **SEE** – Single-event effect
- **SEFI** – Single-event functional interrupt
- **SEU** – Single-event upset
- **SOIC** – Small Outline Integrated Circuit
- **TAMU** – Texas A&M University



# Motivation

- **Limited availability of radiation tolerant flash memories**
- **Radiation performance of state-of-the-art flash is generally good but include some weaknesses**
- **Flash already reaching scaling limits**
- **Resistive random access memory (RRAM) has shown very good tolerance to radiation\***
- **Published radiation test results only from test chips**
- **A first look at the SEE performance of two commercial production-level RRAMs**

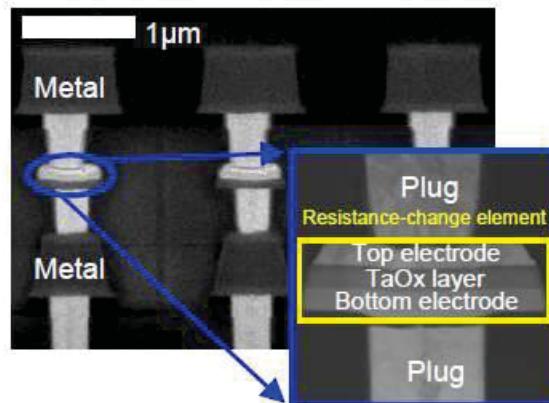
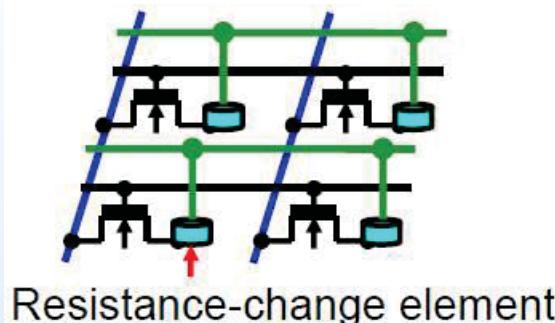
\* M. J. Marinella, S. M. Dalton, P. R. Mickel, P. E. Dodd, M. R. Shaneyfelt, E. Bielejec, G. Vizkelethy, and P. G. Kotula, "Initial assessment of the effects of radiation on the electrical characteristics of  $TaO_x$  memristive memories," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 2987 – 2994, Dec. 2012

H. J. Barnaby, S. Malley, M. Land, S. Charnicki, A. Kathuria, B. Wilkens, E. Delonno, and W. Tong, "Impact of alpha particles on the electrical characteristics of  $TiO_2$  memristors," *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 2838–2844, Dec. 2011.

J. S. Bi, Z. S. Han, E. X. Zhang, M. W. McCurdy, R. A. Reed, R. D. Schrimpf, D. M. Fleetwood, M. L. Alles, R. A. Weller, D. Linten, M. Jurczak, and A. Fantini, "The Impact of X-Ray and Proton Irradiation on HfO<sub>2</sub>/Hf-Based Bipolar Resistive Memories," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 4540 – 4546, Dec. 2013.

# Panasonic Embedded ReRAM

## 1T1R-ReRAM Memory Cell



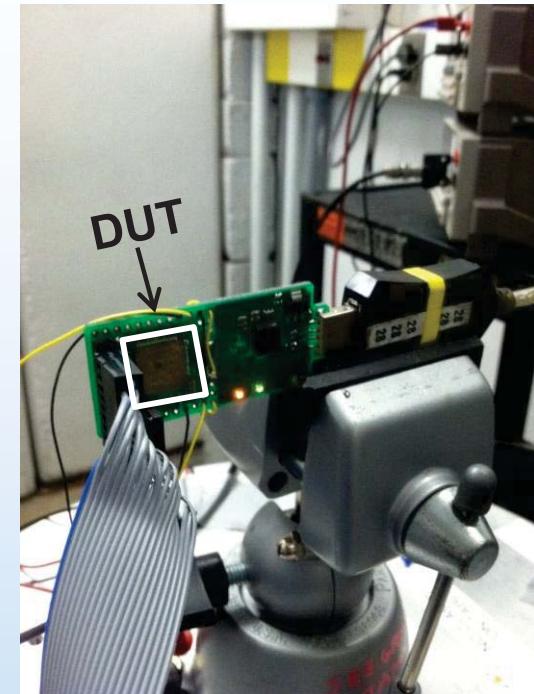
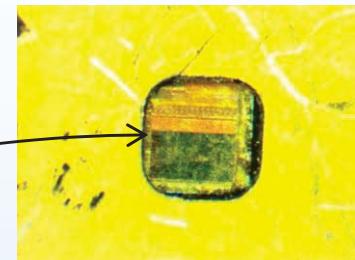
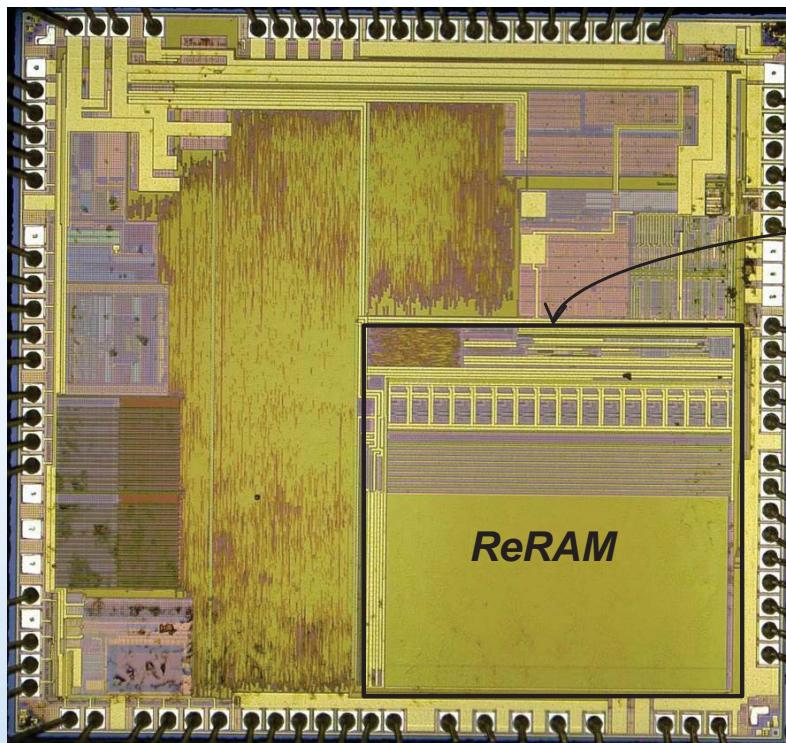
Function	Description
Memory Size	64 KB
Program Endurance	Program area (62 KB): $\geq 10^3$ Data area (2 KB): $\geq 10^5$
Programming Voltage	1.8 to 3.6 V
Reading Voltage	1.1 to 3.6 V
Data Retention	10 years

<http://www.semicon.panasonic.co.jp/en/products/microcomputers/mn101>

ReRAM – Reduction-Oxidation Random Access Memory  
1T1R – 1 transistor 1 resistor

- **Panasonic MN101L**
  - 16 bit microcontroller with embedded ReRAM
  - Industry's first mass production-level ReRAM
- **1T1R array architecture, with CMOS transistor as access transistor to each ReRAM stack**
  - **TaO<sub>x</sub> as switching layer**
  - **Minimum device width  $\sim 0.5 \mu\text{m}$**
  - **Fabricated back-end-of-line in a 180 nm CMOS process**

# Heavy Ion Testing

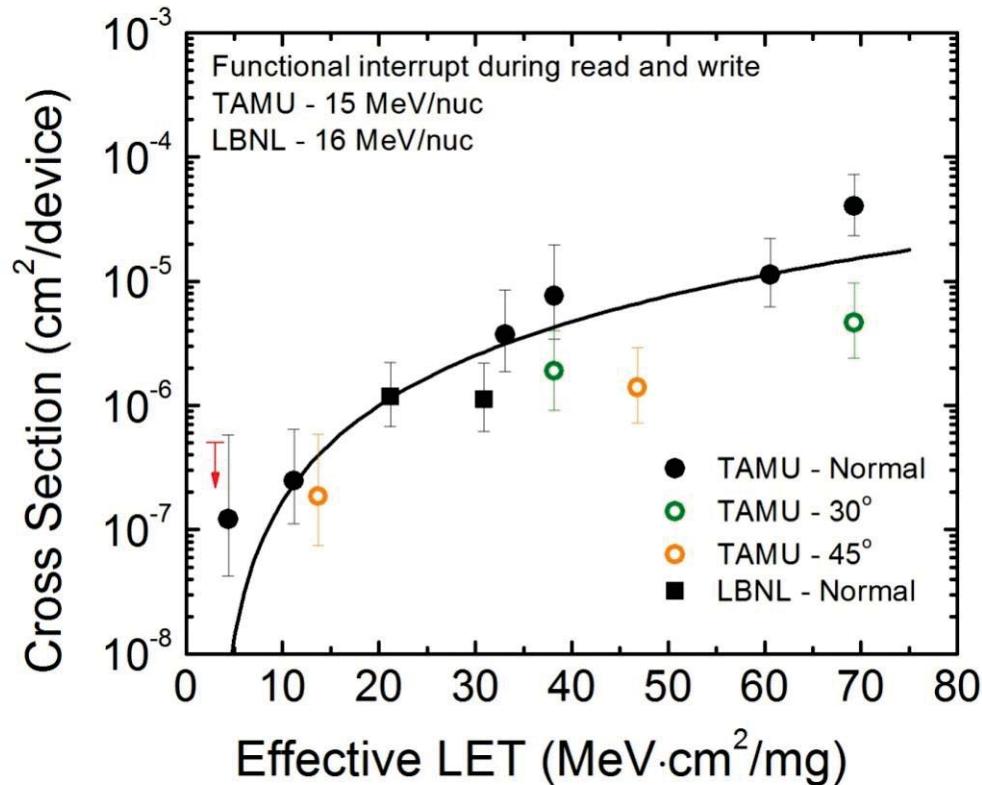


*Microphotograph courtesy of JPL*

- **Kovar lid collimator (254  $\mu\text{m}$ ) exposed ReRAM array and peripheral control circuits**
- **Used Panasonic's evaluation card as test vehicle**
- **ROM operating conditions:  $V_{cc} = 3.3 \text{ V}$ , Frequency = 8 MHz or DC**
- **Test modes: static, dynamic read, read/compare/write, and write**
- **Data patterns: 00, FF, 55, and AA**
- **15 MeV/amu heavy ions in air at Texas A&M University**
- **16 MeV/amu heavy ions in vacuum at Lawrence Berkeley National Laboratory**

ROM – Read-Only Memory

# Heavy Ion Test Results

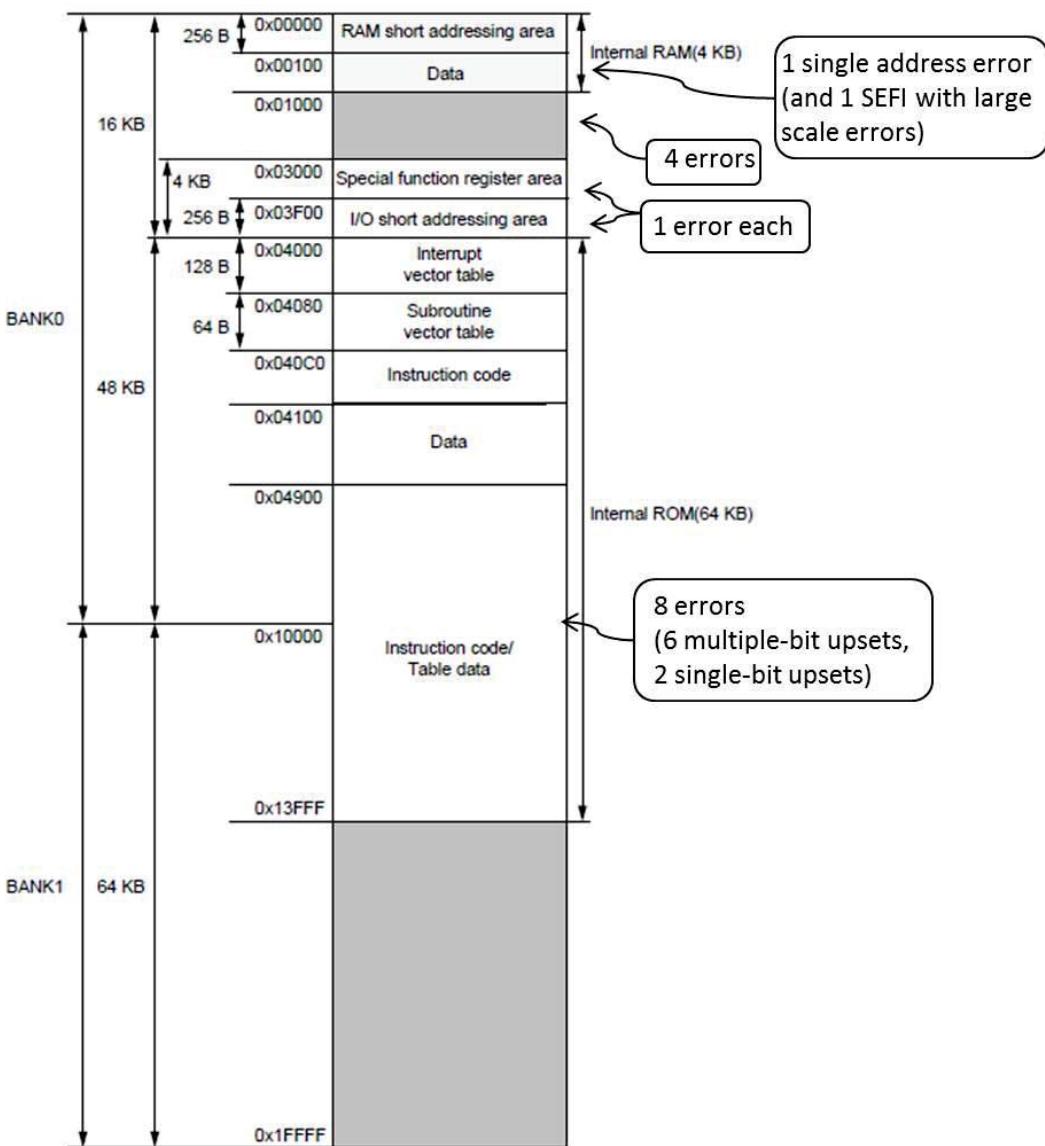


- No SEU from static test
  - 1 functional error following Xe irradiation, during read-back, recovered by a reset
- Dynamic read and write produced mostly SEFIs
  - 1 locked mode event
- Similar SEFI cross sections for read and write test mode
- Angular irradiation
  - Beam shadowing from the collimator likely contributed to reduced cross section

SEU – Single-Event Upset

SEFI – Single-Event Functional Interrupt

# SEE Characteristics



- **Functional interrupts**
  - Microcontroller stops reading/writing
  - Flash vulnerable to large scale page and block errors
- **Bit upsets**
  - Include single-bit and multiple-bit upsets
  - Error address locations distributed throughout the microcontroller memory bank
  - **8 SEUs in the ROM**

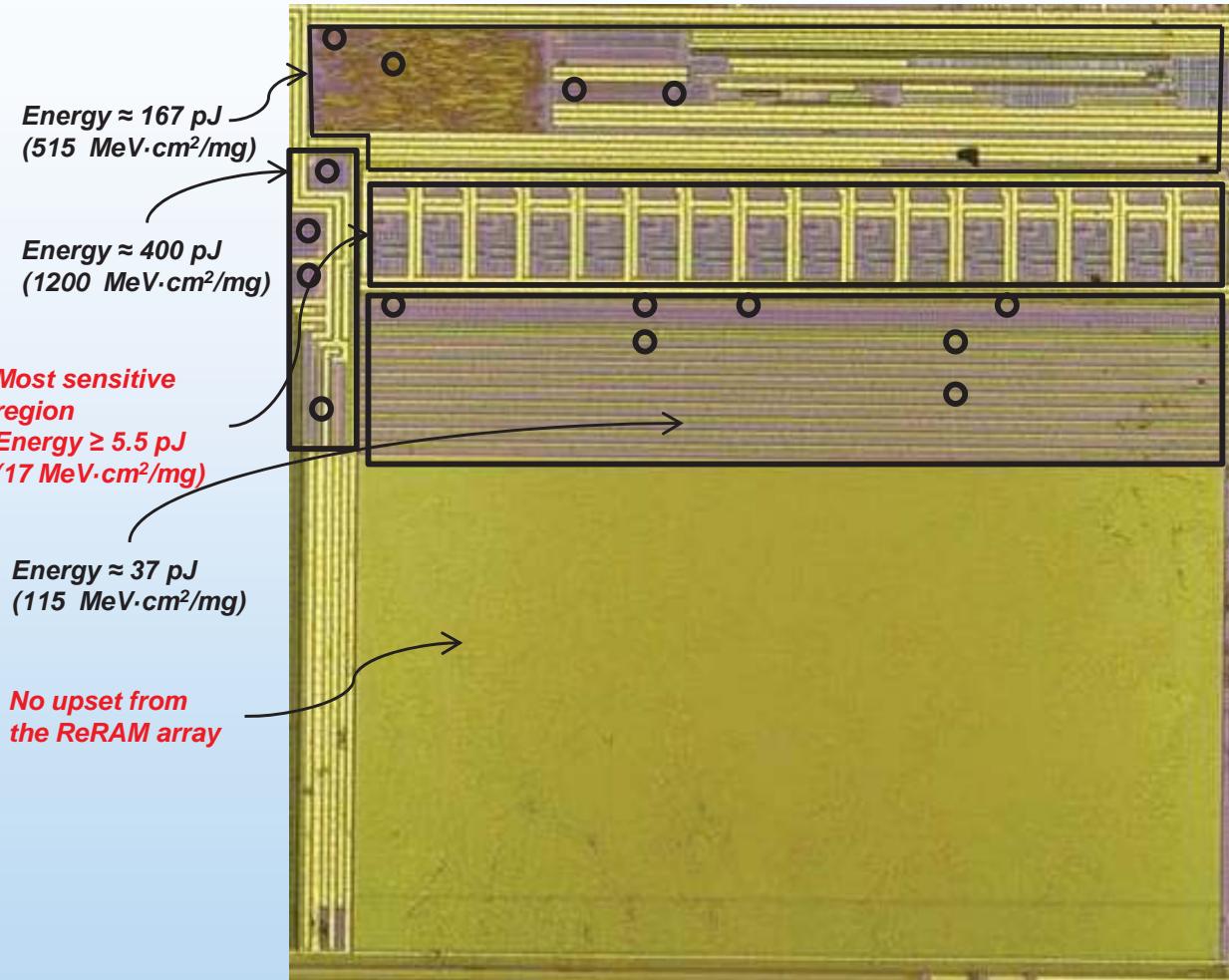


# Pulsed-Laser Testing

- Pulsed-laser testing was carried out at the Naval Research Laboratory
- Laser characteristics
  - Wavelength = 590 nm
  - 1/e penetration range = 2  $\mu$ m in silicon
  - Beam diameter = 1.7  $\mu$ m for 20 $\times$  lens, 0.9  $\mu$ m for 100 $\times$  lens
- We probed the ReRAM array and surrounding peripheral circuits with a 20 $\times$  lens to identify the sensitive regions
- Sensitive areas were further investigated with a 100 $\times$  lens, and the energy was fine-tuned to determine the upset energy threshold
- Equivalent LET values are based on empirical data from previous studies on other device types

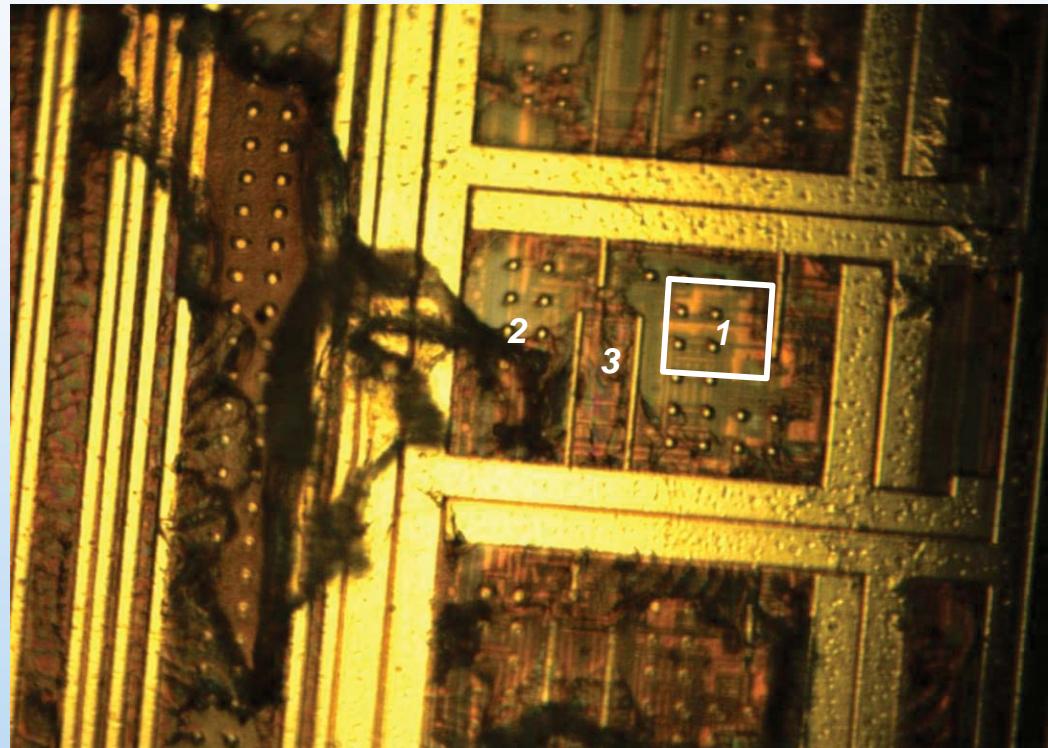
LET – Linear Energy Transfer

# Sensitive Locations



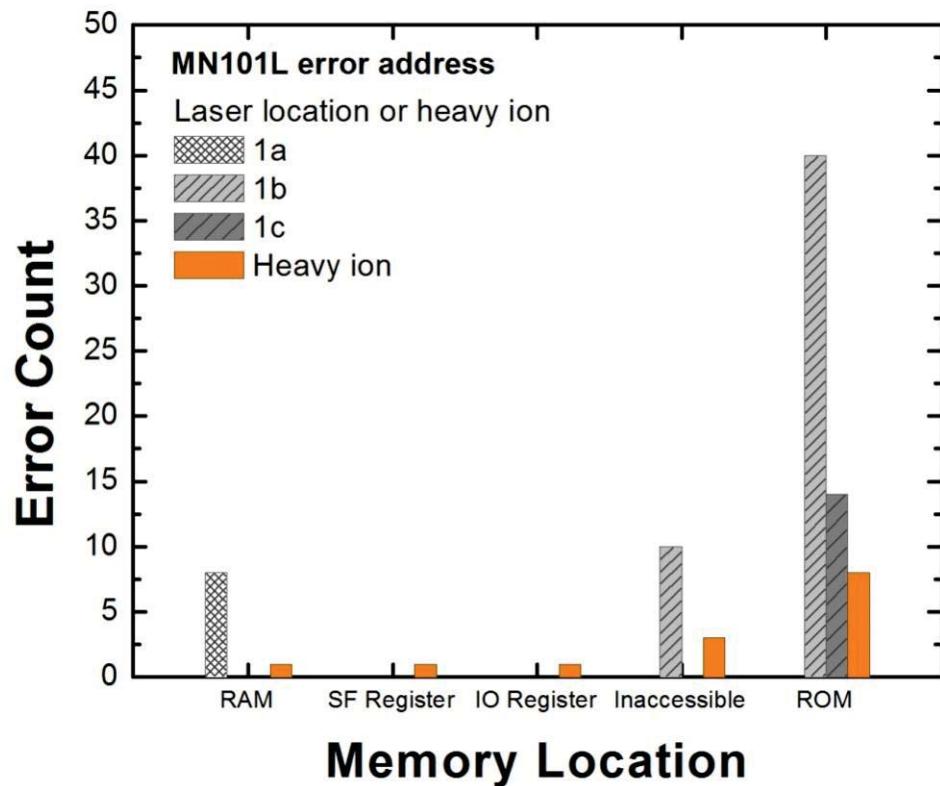
- **Bit upsets**
  - Did not originate from the ReRAM array
  - Location sensitive to SEUs also susceptible to SEFIs
- **Functional interrupt**
  - Stops reading/writing
  - Continuously reading out errors from the ROM
  - Stuck reading at end of Bank0 (FFFF)
  - Continuously reading errors from other address locations beside the ROM

# Upset Sensitivity in the Most Sensitive Location



- Determine upset energy threshold at the most sensitive location using 100 $\times$  lens
- Location 1:
  - Read mode: 5.5 pJ (17 MeV $\cdot$ cm $^2$ /mg)
  - Write mode: 8.6 pJ (26.5 MeV $\cdot$ cm $^2$ /mg)
- Location 2:
  - Read mode: 71 pJ (220 MeV $\cdot$ cm $^2$ /mg)
- Location 3:
  - Read mode: 105 pJ (320 MeV $\cdot$ cm $^2$ /mg)

# SEE Characteristics



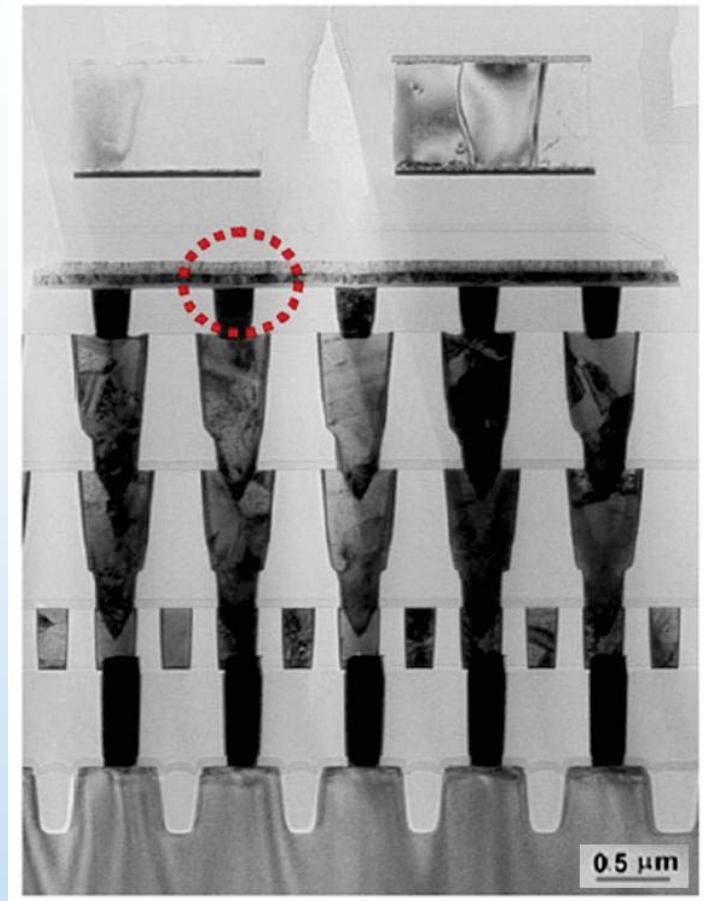
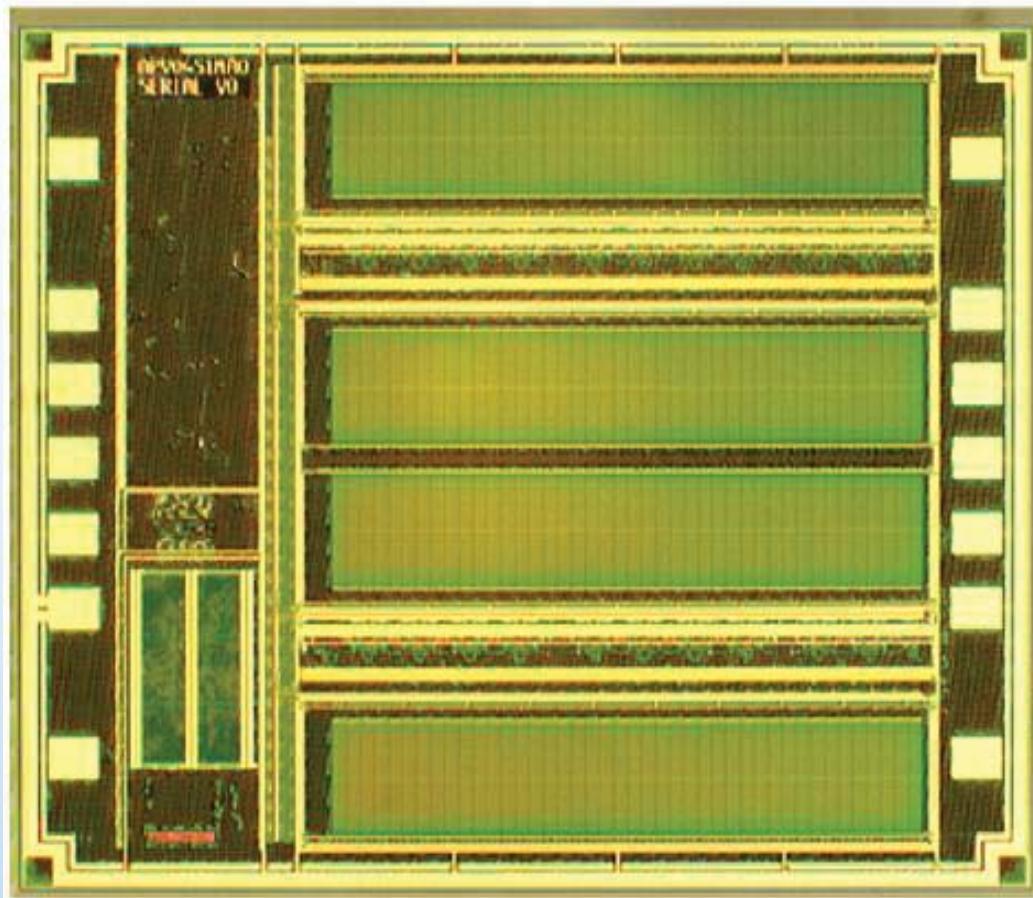
SF Register – Special function register

IO Register – Input/Output register

- **Compare SEE characteristics with heavy ion results**
- **Memory address of errors from laser test are similar to those from heavy ion test**
- **SEFI modes from laser and heavy ion test are also similar**
  - Although limited information was gained from SEFIs that caused immediate cease of operation
- **Sensitive region consists of sense amplifier circuit**
  - SEU in the sensing circuit of flash devices lead to SEFI\*

\* D. Nguyen and L. Scheick, "SEE and TID of emerging non-volatile memories," in Proc. IEEE Radiation Effects Data Workshop, 2002, pp. 62–66.

# Adesto CBRAM

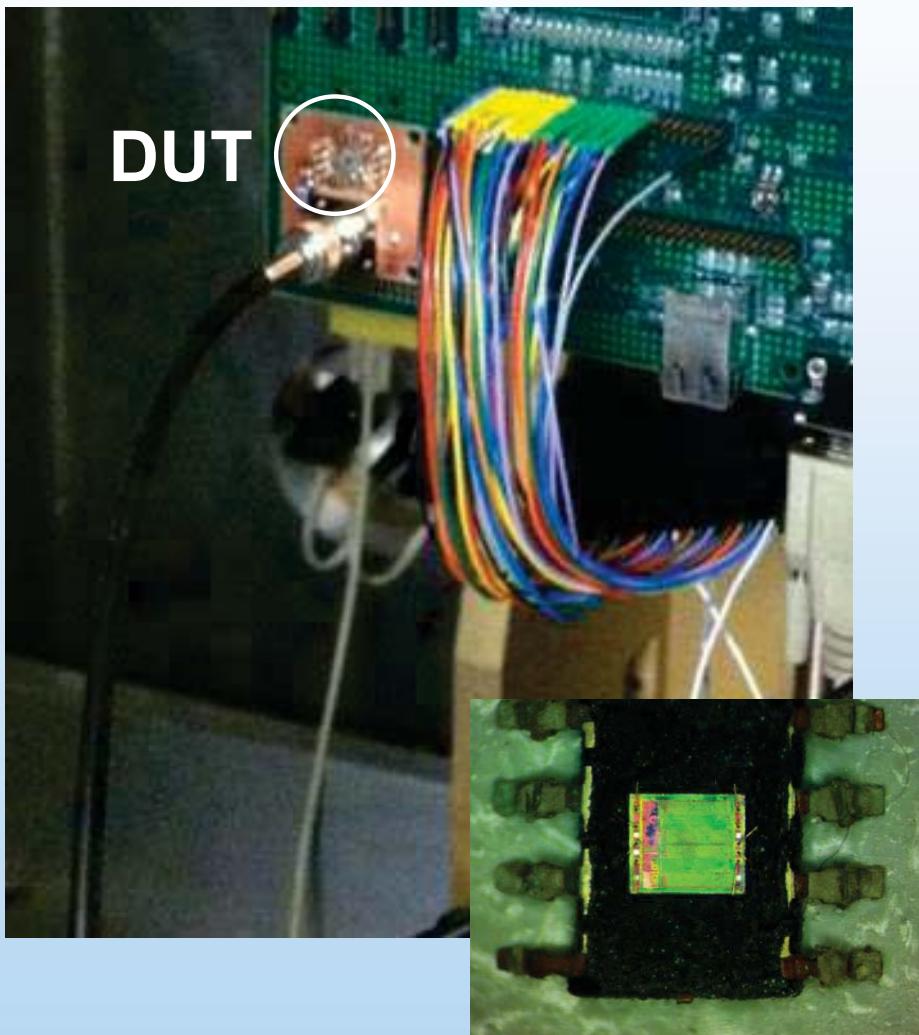


- 128 kb EEPROM from Adesto
- Ag/GeS<sub>2</sub>/W conductive bridge memory (CBRAM)
- 1T1R structure
- Back-end-of-line 130 nm CMOS

EEPROM – Electrically Erasable Programmable Read-Only Memory

To be published on nepp.nasa.gov previously presented by Dakai Chen at the NASA Electronic Parts and Packaging (NEPP)  
Electronics Technology Workshop (ETW), Greenbelt, MD, June 17-19, 2014.

# Adesto CBRAM



- Heavy ion test carried out at LBNL in vacuum
- 8-pin SOIC packages were chemically etched to expose die
- 16 MeV/nuc cocktail
- Test conditions:
  - NASA's LCDT tester
  - $V_{cc} = 3.3$  V
  - Frequency = 1 kHz or DC
  - Mode: static random read, static sequential read, continuous random read, write all/random read, write all/sequential read
  - Patterns: 00, FF, AA, and counter

LBNL – Lawrence Berkeley National Laboratory

SOIC – Small Outline Integrated Circuit

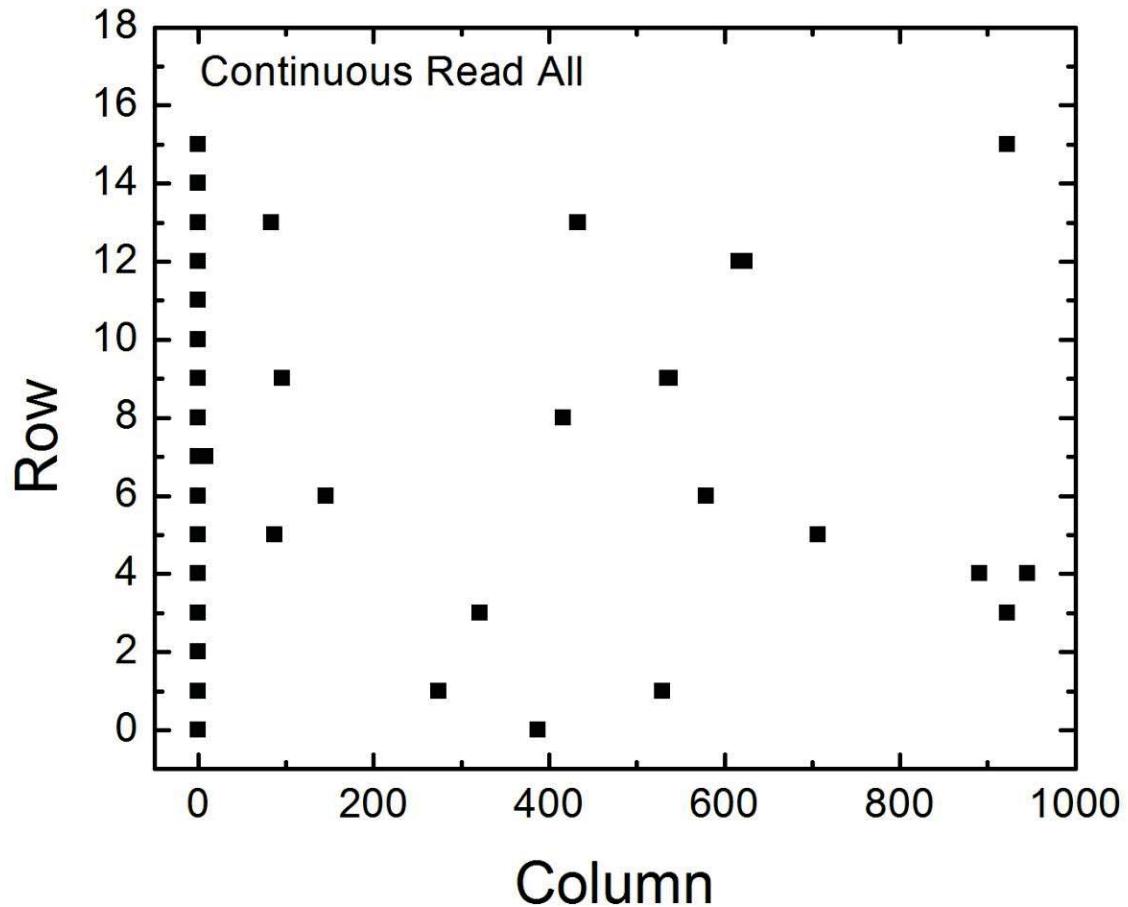
LCDT – Low Cost Digital Tester

# SEE Characteristics



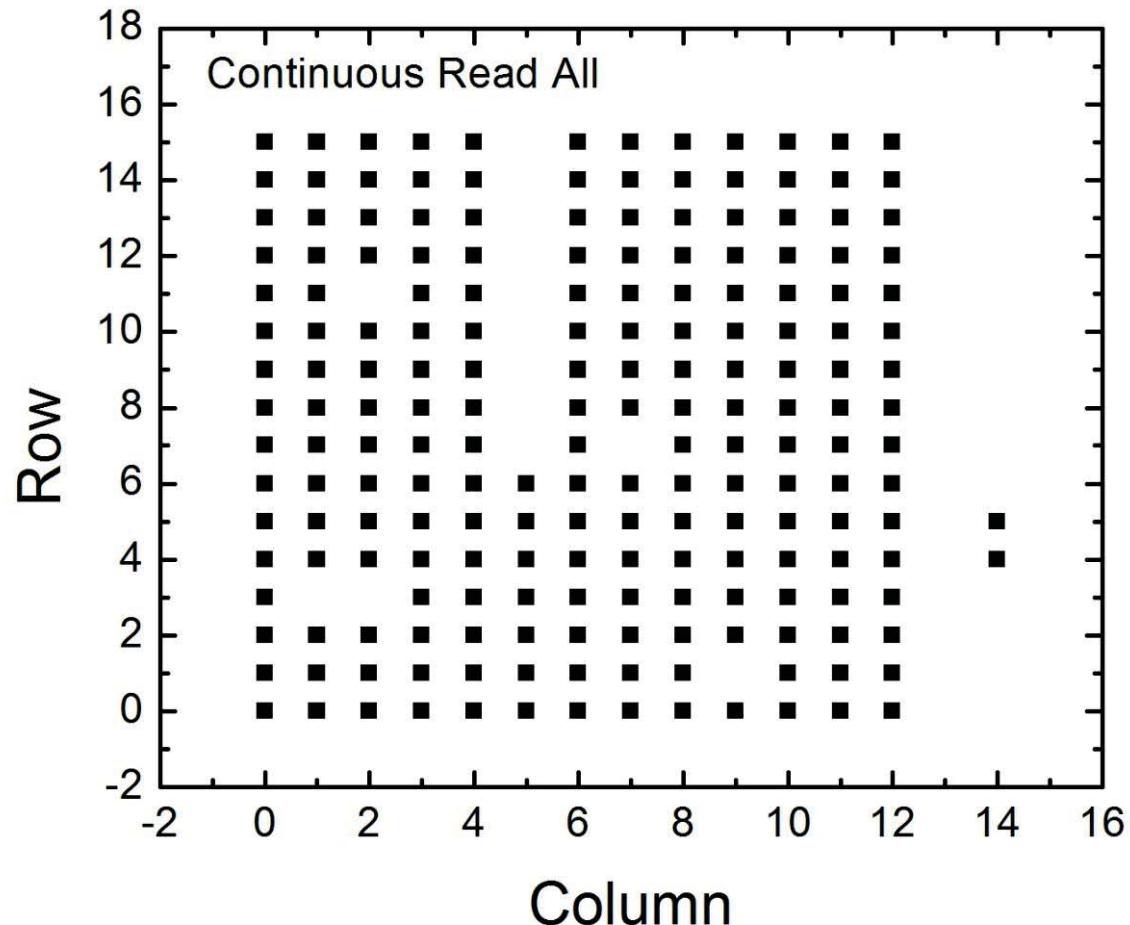
- Static “On” and dynamic test modes produced mostly SEFI
- Most (if not all) bit upsets due to acknowledgement fails, indicative of control circuit errors and not array errors
- SEFI modes
  - Stuck address, accumulating acknowledgement failures
    - Occurred during read and write/read test modes
    - Reset usually required
  - Read errors in continuous addresses
    - Column, page, or entire memory read out 00FF
    - Errors may clear by itself, or reset required
- No Apparent pattern sensitivity for FF, 00, AA, and Counter

# SEE Characteristics



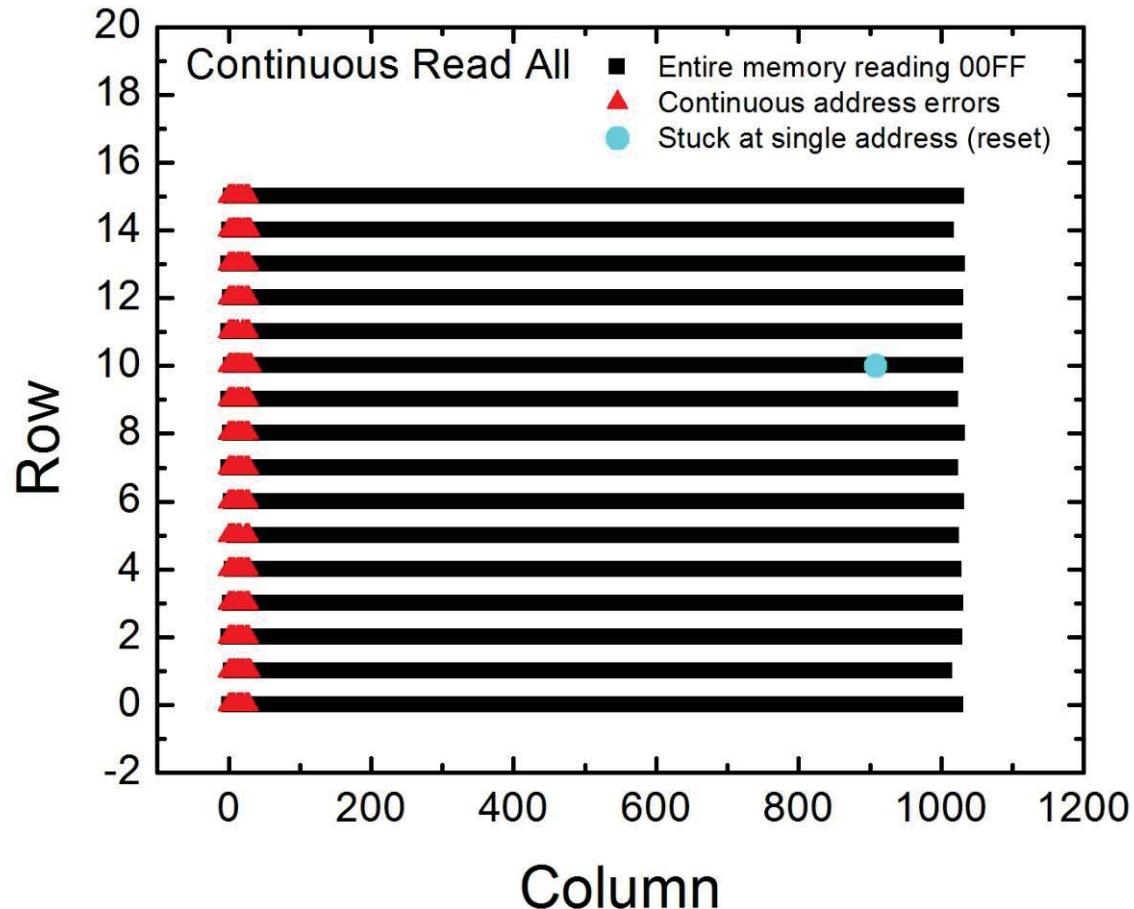
- Column errors (0000 to 000F) during read; memory still functional

# SEE Characteristics



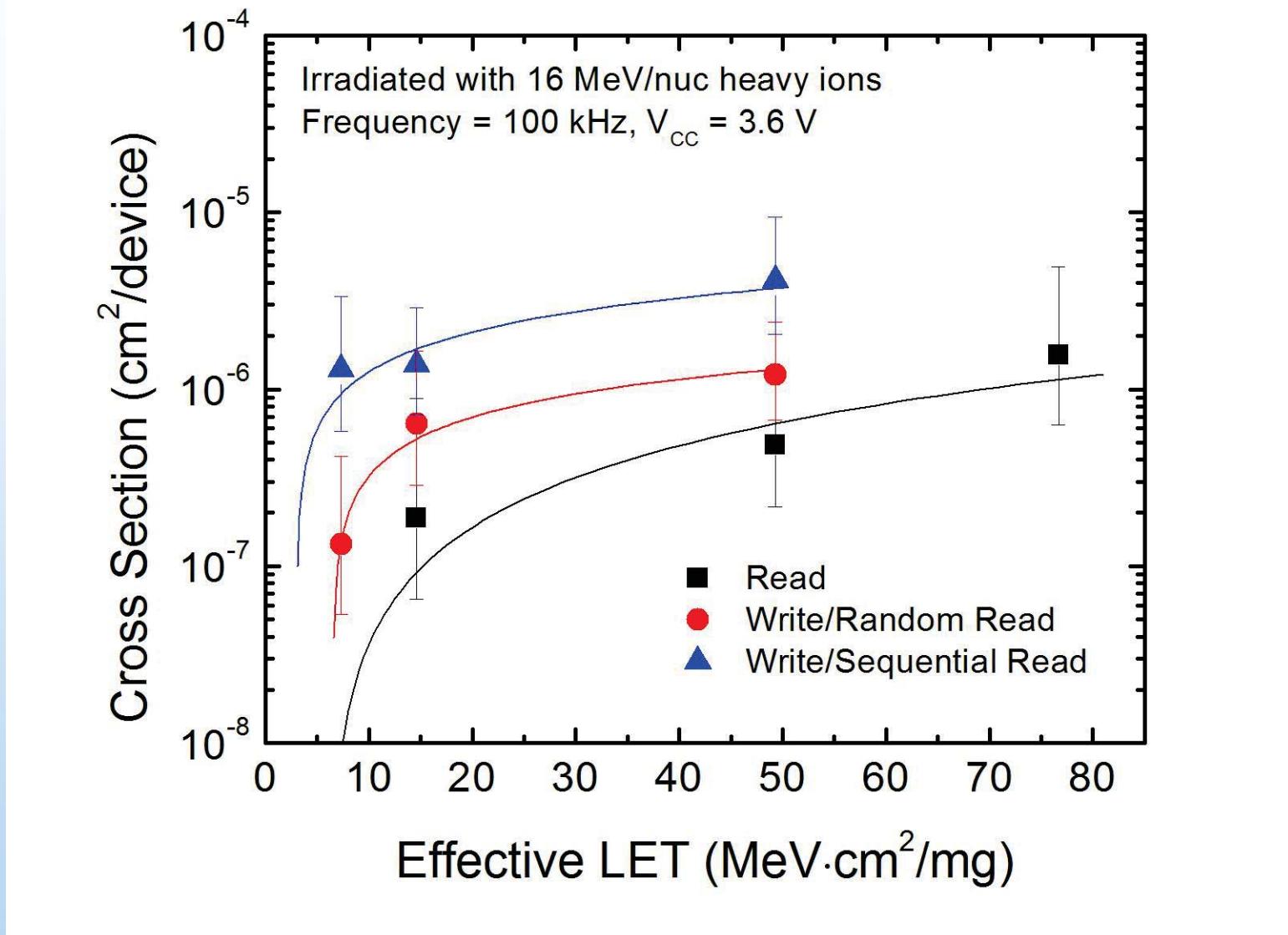
- **Column errors (0000 to 00CF) during read; memory still functional**

# SEE Characteristics



- **Entire memory reading 00FF during read**
- **Column errors (0000 to 00CF) during read**
- **Stuck at single address; reset required**

# SEE Characteristics





# Conclusion

- **RRAM array immune to heavy ions with LET as high as 75 MeV·cm<sup>2</sup>/mg**
  - SEU in CMOS access transistor not enough to cause bit flip
- **SEFI is the dominant error mode**
  - Panasonic MN101L embedded ReRAM's SEFIs originate from sense amplifier circuits
  - Adesto CBRAM showed column/page errors, mass read errors from entire memory, and stuck address errors
- **Lack of charge pump reduces sensitivity to erase or program failure**
  - Eliminates block erase failures (issue for flash)